AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

1. (CURRENTLY AMENDED) An apparatus comprising:

a first circuit configured to generate an upconverted signal in response to an input signal and a first oscillation signal;

a second circuit configured to generate a downconverted signal in response to said upconverted signal and a second oscillation signal; and

a third circuit configured to generate an output signal in response to said downconverted signal and a third oscillation signal derived from said second oscillation signal, wherein said ~~upconverting and said downconverting~~ third circuit is configured to filter undesired channels from said output signal.

2. (ORIGINAL) The apparatus according to claim 1, wherein first circuit comprises:

a low noise amplifier configured to receive said input signal;

a first mixer coupled to an output of said low noise amplifier; and

a first filter coupled to an output of said first mixer and configured to generate said upconverted signal.

3. (ORIGINAL) The apparatus according to claim 2, wherein said first filter comprises an intermediate frequency filter and is further configured to receive said first oscillation signal.

4. (ORIGINAL) The apparatus according to claim 1, wherein said second circuit comprises:

a second mixer pair configured to receive said upconverted signal;

a first summation circuit configured to receive one or more outputs of said second mixer pair; and

a second filter configured to receive an output of said summation circuit and generate said downconverted signal.

5. (CURRENTLY AMENDED) The apparatus according to claim 4, wherein said second mixer pair is configured to receive an in phase signal of said second oscillation signal and a quadrature phase signal of said second oscillation signal, wherein said second ~~filtering~~ filter comprises an intermediate frequency filter.

6. (ORIGINAL) The apparatus according to claim 1, wherein said third circuit comprises:

a third mixer pair configured to receive said downconverted signal;

a second summation circuit configured to receive one of the outputs of said third mixer pair; and

a third filter configured to (i) receive an output of said summation circuit and (ii) generate said output signal.

7. (ORIGINAL) The apparatus according to claim 6, wherein said third mixer pair is configured to receive an in phase signal of said third oscillation signal and a quadrature signal of said third oscillation signal, wherein said third filter comprises a SAW filter.

8. (ORIGINAL) The apparatus according to claim 1, wherein said apparatus is further configured to provide selectivity and gain while not degrading a quality of the input signal.

9. (ORIGINAL) The apparatus according to claim 1, wherein said apparatus is configured to reduce unwanted noise or distortion.

10. (ORIGINAL) The apparatus according to claim 1, wherein said apparatus comprises a single microchip architecture.

11. (ORIGINAL) The apparatus according to claim 1, wherein said apparatus is implemented on a plurality of microchips.

12. (ORIGINAL) The apparatus according to claim 1, wherein said apparatus comprises a tuner.

13. (ORIGINAL) The apparatus according to claim 6, wherein said third mixer comprises an image reject type mixer.

14. (CURRENTLY AMENDED) An apparatus comprising:

means for generating an upconverted signal in response to an input signal and a first oscillation signal;

means for generating a downconverted signal in response to said upconverted signal and a second oscillation signal; and

means for generating an output signal in response to said downconverted signal and a third oscillation signal derived from said second oscillation signal, wherein said ~~upconverting and said downconverting~~ means for generating said output signal is configured to filter undesired channels from said output signal.

15. (CURRENTLY AMENDED) A method for filtering undesired channels from an output signal, comprising the steps of:

(A) generating a ~~downconverted~~ upconverted signal in response to ~~said~~ an input signal and a first oscillation signal;

(B) generating a downconverted signal in response to ~~said~~ an upconverted signal and a second oscillation signal; and

(C) generating said output signal in response to said downconverted signal and a third oscillation signal derived from said second oscillation signal.

16. (ORIGINAL) The method according to claim 15, wherein step (A) comprises:

receiving said input signal by a low noise amplifier;

coupling a first mixer to an output of said low noise amplifier; and

coupling a first filter to an output of said first mixer to generate said upconverted signal.

17. (ORIGINAL) The method according to claim 16, wherein said first filter comprises an intermediate frequency filter and said first mixer is further configured to receive said first oscillation signal.

18. (ORIGINAL) The method according to claim 15, wherein step (B) comprises:

receiving said upconverted signal by a second mixer pair;

configuring a first summation circuit to receive one or more outputs of said second mixer pair; and

configuring a second filter to receive an output of said summation circuit to generate said downconverted signal.

19. (ORIGINAL) The method according to claim 15, wherein step (C) comprises:

configuring a third mixer pair to receive said downconverted signal;

configuring a second summation circuit to receive one outputs of said third mixer pair; and

configuring a third filter to receive an output of said summation circuit to generate said output signal.

20. (CURRENTLY AMENDED) The method according to claim ~~19~~ 18, wherein said second mixer pair is configured to receive an in phase signal of said second oscillation signal and a quadrature phase signal of said second oscillation signal ~~and said third mixer pair is configured to receive an in phase signal of said third oscillation signal and a quadrature phase signal of said third oscillation signal in quadrature phase~~.

21. (ORIGINAL) The method according to claim 15, wherein said method is implemented on a single microchip architecture.

22. (ORIGINAL) The method according to claim 15, wherein said method is implemented on a plurality of microchips.

23. (NEW) The method according to claim 19, wherein said third mixer pair is configured to receive an in phase signal of said third oscillation signal and a quadrature phase signal of said third oscillation signal in quadrature phase.